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Multichip Modules Including Processing

A Literature Survey

by Timothy E. Griffin

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Timothy E. Griffin

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U.S. Army Research Laboratory
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In a review of the literature on multichip modules (MCMs), the focus was on the types of MCMs and processes required to fabricate them. The use of MCMs for connecting integrated circuit chips can improve integration density and potentially improve speed, reliability, size, and life-cycle cost, if MCMs are fabricated in sufficient volume. Particular processes produce each MCM type. Each MCM type has advantages and drawbacks. Known good dice (or chips), proper design, and adequate production volume must be evaluated for each fabrication approach.

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1. Introduction

This report surveys the literature on multichip modules (MCMs) for packaging and interconnecting multiple integrated circuits. It discusses processing, materials, and problems with obtaining known good dice (KGD), and briefly reviews testing problems. Packaging for integrated circuits seeks to support their speed, input/output (I/O) count, reliability, and cost. After an Si integrated circuit or chip is fabricated and tested, the MCM approach to packaging may be considered. This technique, which uses planar and multilayer large-area processing, achieves denser electrical interconnection and better mechanical support of a set of chips than traditional single-chip packages can [1–3]. For advanced proposed circuits, MCMs may approach the speed and one-third the density of integrated circuits, which reduces the size and weight of packaging. MCM techniques increase the interconnection densities notably and may increase both the overall reliability and the speed of circuits. With proper design, the heat dissipation of the mix of chips may be better controlled. The MCM approach can also reduce the size, weight, parts count, and connectors required by the system design. Most MCM fabrication techniques can improve resistance to moisture, acceleration, and environmental effects.

MCM advocates are usually optimistic about the potential of MCMs but do not yet claim that MCMs are ready to take over much of the packaging market. MCMs at this time are aimed at custom circuit designs. There is still limited experience with and knowledge of this design approach, its tradeoffs, and actual production. The supporting processes and fabrication experience are not structured for ready, routine use. The total manufacturing equipment requirements are not minor.

Although it is not mentioned in the literature, we can imagine a generic common carrier design for up to some maximum number of multiple chips. Inclusion of more of a particular type of chip would increase the size (as of random access memory, cache memory, or number of processors) or the feature level. The MCM would be made with these and sealed, so additional chips would be outside that MCM. Such an approach would offer the advantages of MCMs to at least part of a system design.

2. Basics of MCM Design

An MCM provides high-density interconnections between usually bare active chips mounted on a supporting substrate and packaged as a group [4,5]. MCMs can give a higher density of chips, with shorter interconnections, for a major portion of a system than can other packaging schemes. Between chips, usually in one layer, four or more layers of metal interconnections are connected by vertical vias and separated by dielectric layers. A distinctly high 20 to 30 percent of the substrate area is covered by chips, as opposed to 1 to 5 percent in traditional printed wiring board (same as printed circuit board (PCB)) technology. Interconnection density and coverage between chips is typically high. There are generally at least 100 I/O leads to the MCM substrate package.

MCMs have been described as "multiple bare chips attached to a common high-density substrate and packaged as a single interconnected group" [6]. The entire MCM is a sealed unit, not individual chips exposed to the environment. The most complex MCM-D (deposited dielectric) in 1990 was valued at $386. In the year 2000, this amount is projected to be about $71.

In contrast, the older hybrid approach involves a package that contains at least an active semiconductor device and another component, usually on a thick-film or a thin-film substrate, and the associated passive devices needed for functionality. Hybrids emphasize passive devices and thicker interconnections, which do not readily permit circuit density. MCMs were first widely used in packaging for high-density telecommunication and computer systems [7].

Chips are attached flat on the MCM substrate, but to reduce propagation delay they may be stacked onto other layers. Chips could have all I/O pads along one edge; laminated with epoxy spacers into a single unit, such chips can also be flip-chip mounted on that edge by solder bumps. This approach is particularly attractive for memory, with its associated lower power dissipation. Chips can also be attached with tape-automated bonding (TAB) and laser-deposited interconnections.

For this discussion, thick and thin films are defined by the following characteristics: Thick films are conductive, resistive, or insulating and are screen printed on insulating substrates such as 96-percent alumina. The substrates are fired at high temperature before the chips are attached. Thin films are usually photoimaged with photoresist and then selectively etched. Of the three typical layers, the bottom is used to form resistors and is used as an adhesion-promoting layer with the substrate; examples of this are nichrome or tantalum nitride (TaN). The middle layer is a dielectric such as polyimide. The top layer is a conductor such as electroplated Au on a thin seed layer, which is typically sputtered Au. Au is convenient for attaching leads by wire bonding and resists hostile environments.

2.1 MCM Types by Substrate

The four technologies for fabricating MCMs are defined by substrate type. These types are MCM-L (laminate), MCM-C (ceramic), MCM-D (deposited dielectric), and MCM-Si (silicon), which is similar to MCM-D. These are the basic categories, but actually there is a continuum of MCM technologies. MCM-L is the simplest approach, typically using smaller interconnections than the normal PCB techniques [8]. This approach also sometimes uses thin-film conductors. MCM-C is thick film on cofired (with the screened paste) ceramic substrate. This technology is similar to single-die ceramic packages and hybrids. MCM-D uses thin-film metal layers and deposited dielectrics. MCM-D substrate may be ceramic or metal with a dielectric film. MCM-Si has single-crystal Si substrate and usually Al or Cu conductors and silicon dioxide dielectric.

2.2 Interconnections

Several approaches may be used for interconnections. External or first-level connections may be wire-bond, TAB, flip-chip, and/or even flip-TAB for increased density. A flip-chip adhesive underfill may be used for solder-ball connections to spread thermal stress for increased reliability. This also provides lower inductance and noise [9]. The flip-chip technique may have an overlying structure to remove heat from the back; flip-chip and flip-TAB may have a final epoxy in the cavity above the substrate to enhance heat conduction [10]. First-level connections are between the chip and the common circuit base, which is the substrate in chip-on-board technology (bare chips wire-bonded to a PCB) and in MCM-L. When multiple layers are used, the common circuit base has the signal interconnection circuits as well as the power and ground distribution levels.

The second level of connections is to the PCB. Here there may be a heat sink, mount, and transition from the MCM I/O to a larger pitch. A flip-chip connection has a size of fan-out to the wiring plane of only up to two times the die dimension and is reworkable [11]. Flip-chip has a connection failure rate in computers of $10^{-13}/(3600\ \text{s})$, while wire bond is 1000 times that failure level. Thermocompression TAB or wire bonding has a typical fan-out size of four times the die dimension. The relative failure probabilities of contact bonds after 6×10^8 s (20 years) are 10^{-3} for mechanical connections, 10^{-4} for surface mount solder joint, 10^{-6} for wire bond or TAB, and 10^{-8} for connection to Si [5].

TAB is available for all types of MCM and permits device burn-in and testing at speed before assembly. This type of connection bonding is smaller, higher performance, and more expensive than wire bonding. In a process being developed for a TAB pitch of 100 μm to as small as 25 μm, laser light directed down fiber optics energizes a closed tip, for solderless metal-to-metal diffusion at the lead-to-pad interface [12].

2.3 Comparisons

MCM-C is either high- or low-temperature cofired ceramic (HTCC or LTCC). The relative dielectric constant is the ratio of the material dielectric constant ε to the dielectric constant of vacuum ε_0, or $\varepsilon/\varepsilon_0$. Table 1 compares MCM types, in some cases for the highest such performance processing.

The substrate I/O for MCM-D Si is by peripheral contacts, and for other MCM types may be by peripheral contacts and array contacts. The vendor base for MCM-L is large, for MCM-C is medium, and for MCM-D is small. Potential applications for MCM-L are broad, for MCM-C HTCC are claimed as medium, and for the rest are limited, at least with present technology. Technology for MCM-L and MCM-C is mature and for MCM-D is less mature.

Table 1. Characteristics of MCM basic types.

Type	$\varepsilon/\varepsilon_0$	Signal layers	Linewidth (μm)	Spacing (μm)	Via dimensions: Diameter (μm)	Via dimensions: Grid (μm)	Via dimensions: Pad/ diameter	Bonding pad (μm)
MCM-L	3–5	≤15	75–150, ≥60 [a]	40–75	150–200	1250 [a]	1.5	200–250
MCM-C								
HTCC	9.6	—	200–300	100–150	—	—	—	—
LTCC	4.8–8	≤50	100–150, ≥75 [a]	50–75	125, 50–100 [a]	125–450 [a]	—	—
MCM-D	2.4–4	5–10	100–150	50–75	25–75	—	—	—
MCM-Si	3.5–4	≤5	10–75, ≥8 [a]	5–30	15, 8–25 [a]	25–75 [a]	—	—

Type	Pinout grid (μm)	Metal layers	Thermal conductivity (W/cm°C)	Area (cm^2)	Tooling and setup cost	Cost: Low volume	Cost: High volume
MCM-L	2540	1–50	≤0.15	6–500	Low	Low	Low
MCM-C							
HTCC	—	—	—	≤225	Low	Medium	Medium/high
LTCC	Staggered, 1000–2540	1–75	0.20–3	≤225	High	Medium/high	Medium
MCM-D	—	1–9	—	≤100	Medium	High	Medium
MCM-S	Peripheral, 630	1–8	0.5–1.5	≤200	High	High	High

[a]Values reported by Tummala [11]

3. Types of MCMs

Substrate materials have a range of properties. Tables 2 and 3 give some of them.

A new, very advanced substrate becoming available is the Norton Co. DiamaTorr™, a 12.7-cm-diameter diamond substrate with a high thermal conductivity of 20 W/cm°C; it is also electrically insulating. The coefficient of thermal expansion (CTE) of diamond is 1×10^{-6}/°C. This substrate has the potential for three-dimensional use, with numerous stacked layers and two faces as heat sinks, or possibly with liquid cooling. Another substrate is a strong diamond-Cu-Ag alloy, which has a high thermal conductivity of 4.2 W/cm°C, compared to 1.5 for Si; further development may increase this value [13]. The CTE can be matched almost to that of Si.

3.1 MCM-L (Laminate)

MCM-L extends chip-on-board technology. In MCL-L, chips are usually limited in number and they are wire bonded thermosonically out to the

Table 2. Characteristics of MCM substrates and dielectrics.[a]

Characteristic	$\varepsilon/\varepsilon_0$	CTE[b] (10^{-6}/°C)	Fabrication maximum (°C)	Thermal conductivity (W/cm°C)
Aluminum nitride (AlN)	8.8	6.6	1600	typical 2
Mullite + glass	5.9	3.5	1200	0.06
Borosilicate + alumina	5.6	4	900	0.06
Lead borosilicate + alumina	7.8	4.2	900	0.06
Glass-ceramic	5	3	950	0.07
Composite SiO_2 + glass	3.9	1.9	900	0.04
Epoxy resin	4.7	140	200	0.001
Polyimide resin	4.7	75	300	0.001
Maleimide-styril resin	3.7	68	250	0.001
Polyimide PMDA-ODA[c]	3.5	25–40	400	0.002
Polyimide BPDA-ODA[d]	3.0	2–6	400	0.002
Benzocyclobutene	2.7	65	350	0.002
Polyphenyl quinone (PPQ)	2.7	35	450	0.002

[a]Values reported by Tummala [11].
[b]Coefficient of thermal expansion.
[c]Pyromellitic dianhydride oxydianiline.
[d]Biphenyl tetracarboxylic dianhydride oxydianiline.

Table 3. Some MCM-C and MCM-D substrates.

Substrate	$\varepsilon/\varepsilon_0$ at 1 MHz	$\varepsilon/\varepsilon_0$ at 1 GHz	Dielectric breakdown (V/cm)	Thermal conductivity (W/cm°C)	CTE[a] (10^{-6}/°C)
Alumina	9.4 (10.7 at 9.9 GHz)	10.1	770	0.367	6.7
Beryllia	6.9 (5.74 at 8.6 GHz)	6.8	230	2.5	7.5
Glass	—	5.84	—	0.017	4.6
Quartz	3.83 (3.82 at 6 GHz)	—	410	0.014	0.49
Sapphire	— (9.39 at 10 GHz)	9.39	190	0.417	5.6 (parallel to *c*-axis) 5.0 (perpendicular)

Substrate	Bulk resistivity (10^{10} Ω/cm)	Thickness (cm)	Tensile strength (10^8 Pa)	Surface finish (μm)
Alumina	3.16	0.25–1	—	1
Beryllia	10,000	0.635	1.6	15–20
Glass	10,000	0.81, 1.63	—	1
Quartz	3.16	—	0.48	1
Sapphire	10,000	—	4	1

[a]Coefficient of thermal expansion.

substrate at room temperature. Substrate types are usually FR-4 epoxy-glass laminate, bismaleimide triazine (BT) epoxy, polyimide, or cyanate ester, all in E-glass fabric (see table 4). A few epoxies are photoimageable. The $\varepsilon/\varepsilon_0$ is usually low for interconnection speed; a number as low as feasible is desired. Reliability is usually better for a higher glass transition temperature, T_{glass} [14]. Subsequent processing must not reach this glass transition temperature. The CTE, particularly in-plane, must be close or equal to that of nearby materials.

There are between six and eight layers on the typical MCM; two are for signals, and the others are power, ground, and distribution or pad, which is Au for wire bonding. The ground plane is at least 13 μm thick. Simple "C" stage laminate is 0.0106 cm thick, and single-ply prepeg (partially cured with sheet or resin in fabric) is thinner; when these are combined, even 10 to 12 layers are thinner than 0.16 cm.

PCB technology has Cu foil on plastic laminate dielectric, which is glass fabric with epoxy resin. MCM-L adds the etching of thin conductors to a 76.2-μm width and excimer laser drilling or ablation of vias as small as 152.4 μm across. Cu can also be electroplated economically, such as through a 3-μm-linewidth photoresist mask, or can be electroless (catalytically) plated on a seeding layer. Bonding can have 10-μm wires on 40-μm pitch; a 3500-μm length has a controllable, low 175-μm height. Chips may be mounted on both sides of the substrate.

MCM-L laminates generally have poor heat conduction. The CTE of an Si die is 2.6×10^{-6}/°C and generally does not match that of the substrate. MCM-L is most often used in computer workstations and small equipment to 100 MHz with up to 25 chips, most of them memory chips.

MCM-L is low cost and often cost-effective [14]. For a density not available with PCB, four layers with 100-μm lines and spaces and 300-μm vias can cost \$0.15/cm^2 (compare MCM-C at \$1.5/cm^2 and MCM-D at \$15/cm^2). Chips can generally cover up to 40 percent of the substrate. The laminates

Table 4. MCM-L typical substrates.

Substrate type[a]	$\varepsilon/\varepsilon_0$ At << 1 MHz	$\varepsilon/\varepsilon_0$ At 1 MHz	Dielectric loss at 1 MHz	CTE[b] (10–5/°C) In plane	CTE[b] (10–5/°C) Out of plane	T_{glass} (°C)	Relative cost
FR-4 epoxy	4.8[c]	4.5	0.03	1.6	8	125	1
BT epoxy	4.2[c]	4.1	0.02	1.4	7.5	180	1.8
Polyimide	4.5[c]	4.5	0.01	1.3	7	250	3.5
Cyanate ester	4.5[c]	—	—	1.5	—	230	4.5
PCL 511[d]	—	3.46	0.0003	1.5	8.5	190	—

[a]All substrates are in E-glass fabric; resin content is 45 percent.
[b]Coefficient of thermal expansion.
[c]Resin content is not reported; probably 45 to 50 percent.
[d]Resin content is 50 percent.

used in this process do not generally fracture very easily. The MCM may have perimeter pads for edge connection or pins, or have lands on the bottom for ball-grid array or pin-grid array connections. Epoxy overmolding or liquid-epoxy encapsulation is compatible with outside interconnections. The substrate may be the final package interconnection and may not need environmental protection. Assembly may be automated for quality, reliability, and lower cost. Chips are often bonded with epoxy having high strength and little hydrolyzable chlorine to corrode metallization. Power dissipation may exceed 0.32 W/cm^2 without thermal vias such as Cu or, sometimes, insulating SiO_2.

An emerging technology, MCM-L/D is defined as using MCM-L processing for most steps and a layer or more of surface MCM-D processing for more performance. It has interconnections with 25-μm linewidth and 50-μm vias, as opposed to MCM-L's 75- and 150-μm, respectively. Obviously a design with its accompanying performance and cost could be tailored, rather than the designer's having to accept one of these two very different values.

In MCM-L, thermal fatigue of the plating metal of plated-through via holes, caused by out-of-plane expansion, presently limits the lifetime. FR-4 substrates with 10 layers and 330-μm vias survive an impressive 100 cycles from –65 to 125°C. Epoxy liquid encapsulants with more than 60 percent by weight fused silica (CTE 5×10^{-7}/°C) have their CTE reduced to 10^{-5}/°C, reducing distortion of larger areas. A silicone gel has been suggested outside the epoxy for chemical and moisture protection. MCM-L may be larger than other MCM.

3.2 MCM-C (Ceramic)

MCM-C consists of hybrid circuits on a ceramic substrate with bare chips and screen-printed interconnections. Substrate materials may be 96- or 99.5-percent alumina, or 99.5-percent beryllia (BeO). For 99.5-percent alumina, $\varepsilon/\varepsilon_0$ to 1 GHz is about 9.8, and the dissipation factor is 4×10^{-4}. The thermal conductivity is 0.367 W/cm°C at 25°C and 0.187 at 300°C. The CTE to 300°C is 6.6×10^{-6}/°C. Tensile strength is 1.93×10^8 Pa (28,000 lb/in.^{2}). Surface finish is 0.1 μm RMS.

In MCM-C, green (unfired) dielectric sheets of alumina powder, glass, and organic material are formed and dried; vias and screen-printed conductors are imprinted. From this parallel process, acceptable sheets are then stacked, aligned, and laminated at temperature and pressure. With high alumina content, HTCC is fired at 1600°C, which allows only the use of W and Mo-Mn as conductors. HTCC has shrinkage and few options. LTCC fired at 850°C permits Au, Ag, and Cu as conductors; the dielectric is alumina-filled glass or crystallized ceramic. Chips are attached by flip-chip or perhaps in individual carriers. Shrinkage during firing affects dimensional control; this restricts reduction of dimensions. LTCC may have a beneficially low $\varepsilon/\varepsilon_0$. Resistors, capacitors, and inductors may be buried [9] in the substrate. Ball grid arrays have larger solder bumps to attach the package to the PCB. Speed may exceed 100 MHz with proper design.

MCM-C is used in mainframe computers and some military systems. In general, for corrosion protection, Cu may be coated with Cr or electroless Ni, but at high frequency the system sees this coating's higher resistivity, because the skin depth restricts the current toward the conductor's surface.

MCM-C can have higher density interconnections with a thick-film photosensitive conductor and dielectric, such as Dupont's Fodel™ [15]. This can be fabricated into a 20 × 20 cm double-sided memory module with seven conductive layers. The dielectric is LTCC, 20 μm thick per application; two applications give a 40-μm layer, which may have a 50 × 50 μm via. The dielectric fires to become a glass-ceramic. A conductor 9 μm thick can have a linewidth of 25 μm with 50-μm spaces; it fires to a ceramic-metal, so humidity does not corrode it. Table 5 has electrical and thermal comparisons of MCM types. A top conductive layer is generally used for protection from moisture.

3.3 MCM-D (Deposited Dielectric) and MCM-Si

MCM-D uses some of the complex and expensive high technology of integrated circuits. Thin-film interconnections are layered between deposited polymer dielectrics or plasma-enhanced chemical vapor deposited (CVD) SiO_2 on an Si, ceramic, metal, or PCB laminate support. Wet etching of conductors and the polyimide precursor is generally the technique of choice. MCM-D is also fabricated by high-technology techniques associated with chip fabrication, such as plasma etching of organic dielectrics, mechanical polishing for planarity, and similar processing. Compared to chips, MCMs and flat-panel displays have more comparable dimensions and resolutions, and may use similar fabrication equipment with lower price per unit area. Sputtered, evaporated, or electroplated conductors are patterned by photolithography with wet or plasma etching. Liftoff metallization may be used, through a removable organic mask with edges undercut at the opening. Patterning may be by laser deposition. Repairs are performed after each level has been fabricated.

In MCM-D, a polymer such as polyimide, which has a lower $\varepsilon/\varepsilon_0$, reduces capacitive loading. This, along with shorter interconnection paths, permits higher circuit speeds. The CTE of the chip and the Si substrate match.

Table 5. Electrical and thermal comparisons of MCM types [15].

Characteristic	Electrical conductivity (mΩ/square)	Thermal conductivity (W/cm°C)	Dielectric thickness between conductive layers (μm)	Dielectric thermal conductance (W/°C)
MCM-L	0.9 (Cu)	0.2	200	0.17
MCM-C	4 (Au)	3.5	40	0.9
MCM-D (25-μm linewidth)	5 (Cu)	0.2	20	0.33
MCM-Si	6 (Cu) 15 (Al)	4	8	2

Chips may occupy half the substrate. The literature indicates that Si wafer substrate may have unscribed chips fabricated onto the surface for built-in decoupling capacitors or possibly off-chip drivers, voltage regulators, and even memory. The substrate needs a mechanical support structure for strength and does not have foreseeable grid array connections. Conductors of Al are not as highly conductive as is desired at high frequency, so Cu is now being substituted for Al.

A variant of MCM-C, MCM-CD is defined as having one or two layers of MCM-D on top of MCM-C. This type is used for high-speed mainframe computers and is also called IBM's thermal conduction module. That module increases computational performance by increasing heat dissipation and off-chip speed and density, as are required for very-high-speed bipolar digital logic. Mainframe technology has recently changed from biopolar logic to denser and lower powered complementary metal oxide semiconductor. The thermal conduction module is not optimum for other applications; particularly, its metal pistons, which are cooled by He to a metal package with forced air (or earlier water) cooling apparatus, are heavy and difficult to manufacture. The glass-ceramic's CTE is chosen to minimize the maximum solder shear strain. In 1990, two thin-film layers for signal redistribution were on 63 layers of glass-ceramic with Cu. This 12.75×12.75 cm square had 121 chips with 648 interconnections each and 27 W each; smaller linewidths would need fewer layers [11]. Wiring density was 844 cm/cm^2; the bottom had 2772 pins for I/O. This expensive MCM includes engineering-change pads. Versions less intensively cooled but with high performance are used in computer workstations. The function of packaging, including MCMs, is to interconnect, power, cool, and protect the chips. The computer's cycle time is slowed by package and chips; it is easier to achieve 12 ns with MCMs, and achieving 8 ns basically requires MCMs. An MCM can reduce the cycles per instruction. An MCM-CD excluding its chips must be more reliable than those chips in an unpackaged state.

4. Consideration of Advantages for Implementation

With MCM technology, smaller size, higher speeds, and even reduced power compared to other packaging are possible. MCM-D, particularly with flip-chip solder bump connections, makes an I/O negligibly cheap, small, and (if local) low power. Almost all MCM designs are customer-specific; hence, standardization or high volume for low cost is often difficult to obtain, and the cost is higher. The first MCM users sought higher performance, the second users seek reliability or reduced size, and the later users will seek a cost advantage.

MCMs reduce life-cycle cost by reducing the fabrication cost. An additional benefit is the reduction in size and weight. MCM technology consolidates connections from each die to its usual single-die package with connections beyond that package; fewer mechanical connections and shorter interconnections increase reliability [16]. There are notably fewer solder joints for the complexity of the package, and a shorter lid seal. The

reliability is better for monometallic interconnections, which cannot have intermetallic growth problems. The often more controlled and cooler chip temperatures reduce interconnect diffusion and grain growth. More of the electronic systems are sealed from corrosion and environmental concerns. An MCM must be easily aligned and ruggedly assembled into any further packaging or system motherboard. Although MCM materials may be selected for greater thermal conductivity, and although closer chip placement may use less drive power, denser packaging increases the overall power density.

For higher speed, higher interconnection density, and higher power density, the MCM transmission-line I/O has certain requirements [6]. These include an uninterrupted ground, a low parasitic power-supply bus exchanger, and a flexible second-level interface for thermal and electrical interconnections. MCMs in future designs will connect with a plug-in board or with other, stacked MCMs. Such connections could replace backplanes, connectors, and associated circuitry. Preferably, the interconnection line height approaches its width, so the resistance is desirably less than 0.2 times its characteristic impedance [17].

MCMs could be improved if some of the Si chip designs were specifically optimized for MCM use, instead of for the existing single type of package [17]. Additional chips would then be designed to use the improved interconnections of MCMs. MCMs could have an area array of 1000 to 2000 I/Os, without the processing yield failure of wafer scale integration. Chips custom designed for the load of one MCM or of similar MCMs could have faster drive stages because of reduced drive current [10]. For a given Si process, dense integration permits the output drives of one-die leading-edge microprocessors to have only limited capability. In an MCM, chips mounted in closer proximity would have less capacitive interconnection load to drive and hence less power dissipation. Another improvement with MCMs could be one or more additional chips with improved output drives. One-chip microprocessors also contain a limited-size, high-speed cache memory (presently up to tens of kilobytes) and somewhat limited logic. The microprocessor could use one or more chips of high-speed cache memory, with the cache readable within one instruction cycle of the processor for avoiding wait states [10]. The Si area for logic would be larger, potentially far larger.

For a given price and a given Si process, a multichip microprocessor designed for an MCM could give better performance than the one-chip microprocessor version. This assumes that design costs are comparable or are amortized over sufficient volume to be small. Achieving such high volume with MCMs is not likely within a few years; for example, some types of MCM would need a partial redesign to handle a shrunken chip.

Because of advanced interconnections of chips provided by the MCM, an MCM could incorporate application-specific integrated circuits, not necessary replace them. As leading-edge chips tend to become larger, using MCMs to incorporate them is a partial substitute for wafer-scale integration.

5. Processing and Its Materials

The physical structure of an MCM is fabricated with semiconductor processing techniques. Process improvements and the introduction of new materials have been evolutionary. Personnel at the Army Research Laboratory have developed some familiarity with these techniques by processing devices.

Solder can be evaporated through an Mo mask clamped and mechanically aligned with the substrate. This layer is of high purity and has few included voids. Solder can also be electroplated, but with lower purity and possible voids. This process is accomplished through a hot-rolled or vacuum-laminated and patterned Riston™ dry-sheet photoresist mask with a 50- to 75-μm thickness to keep growth vertical, or through photoresist [18]. Corrosion of Al can be a problem with this process.

Electroless plating of Ni below 100°C is planar and gives adequate conductivity and stability beyond 400°C for later processing. For example, selective via filling first etches Cr from Cu in the exposed areas, and then aqueous palladium chloride or evaporated palladium leaves a few atomic layers of palladium as a catalytic surface for self-alignment. A plating solution with nickel chloride and sodium borohydride for Ni/1-percent boron is not too basic for polyimide; this solution plates at a rate of 1.7 nm/s at 60°C.

Compared to the Si chip fabrication process, MCM technology requires photolithography with larger linewidths and a much larger physical area. Patterning systems need a lower numerical aperture for a larger depth of focus compared to wafer processing [17]. A larger depth of focus does not require as flat a surface. Hence, when a typical thickness of 25 μm of photoimageable polyimide is built up in many layers, it would require less frequent planarization.

Advances in processing include additional dielectric materials. SiO_2 cannot be deposited more than 1 μm thick without developing cracks. Over higher topography, MCMs require economical large-area metallization, lithography (50 × 60 cm), and polymer deposition. Divinylsiloxane bisbenzocyclobutene, usually called BCB [19,20], is an organic dielectric tailored for MCM-D and MCM-L. It is either spray coated (so that the maximum fraction of material is used) or, after an adhesion promoter, spun on. Extrusion coating is also mentioned in the literature [17]. BCB's low water absorption eliminates the moisture bakeout steps required for polyimide films. BCB has low stress (25 to 40 MPa) and a CTE of 5.2×10^{-5}/°C, compatible with the usual substrates. BCB has a low $\varepsilon/\varepsilon_0$ of 2.7 independent of temperature, and a low loss of 0.0008 at 1 MHz. At 10 GHz, $\varepsilon/\varepsilon_0$ is 2.58 and loss is 0.002 (polyimide is far lossier).

BCB's formula is 1,3-bis(2-bicyclo[4.2.0]octa-1,3,5-trien-3-ylethenyl)-1,1,3,3-tetramethyl-disiloxane (mixed isomers) with an antioxidant additive. Simply, from a central –O– are two $-Si(CH_3)_2CH{=}CH-$; call all this –R–. To each side of –R– is a benzene-like C_6H_3 ring with, on the far

side, a $-CH_2CH_2-$ closing a ring of four C. Thermally, this becomes an intermediate structure having, connected to –R–, two rings of

$$-C{=}CH-C^{//}{}^{CH_2}-C^{//}{}^{CH_2}-CH{=}C-.$$

Polymerization of this material crosslinks a percentage of the material, producing no volatiles. In a planar drawing of the polymer, to the top of a benzene-like ring of $-CH\backslash CC/CHCH/C-$ is $-CH_2\backslash CHC/HCH_2-$ (clockwise from left, the two "–" close the ring), closing a cyclohexane-like ring of six C. Repeat this two-ring structure to the bottom right of the benzene-like ring. From the first cyclohexane-like ring to the upper left extends $-Si(CH_3)_2-O-$ (giving good thermal stability), and to the upper right is the bottom left of another benzene-like ring.

A 20-μm film of BCB at 350°C in N_2 has a weight loss of 2 percent in 7200 s. If the temperature is ramped at 0.17°C/s, weight loss begins at 417°C in N_2; this stability is usable for MCM fabrication and rework and for permanence below 180°C. When the film is 70-percent polymerized, T_{glass} is 130°C; at 80 percent, it is 200°C; and at 100 percent, it is more than 350°C. By comparison, T_{glass} is 300 to 320°C for some polyimides. This organic dielectric has a distinctly negligible 0.14-percent H_2O uptake, of which three-fourths dissipates in 90 s at 6-percent relative humidity. BCB withstands boiling water for 14,400 s, with adherence maintained on Al or SiO_2; H_2O uptake is 0.25 percent. Moisture uptake increases $\varepsilon/\varepsilon_0$ by less than 2.2 percent typically, by 10 percent in 50-percent relative humidity air at 100°C after 10 years, or at 125°C after a year. Hence BCB does not need to be hermetically sealed in practical use. BCB does not need a transformation such as imidization to become a usable end structure; as applied in a solvent mixture, it is 35-percent polymerized; 210°C in N_2 for 1800 s cures this to 70 percent. It is usually spun, giving 1 to 25 μm. With Cu, it does not need an adhesion glue layer or, unlike polyimide, a diffusion barrier. BCB is not ionic, acidic, or basic. With most of the solvent evaporating during the spin-on, heat treatment shrinks BCB less than 5 percent.

The photoimageable version of BCB crosslinks to stay where exposed, like a negative photoresist, but remains permanently. The one photocrosslinking agent (two for 20 μm) and an antioxidant cause curing to shrink BCB about 10 to 17 percent, which is smaller than polyimide or most organic dielectrics. With rounded 75° walls, sputtered metal would not readily deposit discontinuously or break; 25 × 25 μm vias are patternable in a 10-μm film, or 12-μm lines and spaces in a 5.6-μm film. In the cure cycle in N_2 to 90-percent polymer, the temperature ramps from 50°C to 100°C in 300 s, stays for 900 s, ramps to 150°C in 900 s, stays for 900 s, ramps to 250°C in 3600 s, stays for 3600 s, cools to 100°C in 7200 s, and cools to ambient with low surface stress. Patterning of nonphotoimageable BCB is by O_2-fluorinated plasma etching.

Adhesion of films enables small-geometry fabrication. Before the adhesion promoter for BCB is applied, O_2 plasma treatment for 1800 s for Si wafers with native SiO_2 gives a better film adhesion. To improve the usually difficult adhesion of metal on polymer, the manufacturer will not have cured the BCB above 70 percent [21], and its surface is roughened inherently

when receiving metallization by argon sputtering or when in O_2 plasma treatment. BCB needs the O_2 plasma treatment for evaporated Al to adhere; sputtered metallization is the preferred process. Adhesion of BCB on Al is improved with an adhesion promoter. After two adhesion promoters, BCB adheres on plated or evaporated Au. For Au, an underlying 7.5 nm of Ti gives adhesion to a substrate, and a removable 1.2-nm Ti overlayer holds photoresist, through which Au can be plated [22]. After Cu is treated with dilute acetic acid and adhesion promoter, BCB adheres. BCB adheres well to a previous layer of BCB that has cured less than 80 percent; a target is 70 percent.

The surface topography may not be planar because of patterned conductors, dielectrics, or even placement of components. To planarize, or level, surface topography, BCB is the best material available at this time, since there is relatively little shrinkage from solvent loss or thermal polymerization. Solventless epoxy has low thermal stability; spin-on glass needs thermal processing and cracks if thicker than 1 μm [23]. BCB flows thermally in the planar configuration during polymerization, then during later heating is thermoset, unlike polyimide, which is thermoplastic. In planarization, the height of the overlying feature in the surface of BCB over a line is reduced or flattened by a percentage compared to the height of the line. BCB that is 10 μm thick planarizes an isolated line 4.5 μm high and 50 μm wide by 90.3 percent (flatter); 7.5-μm-thick BCB planarizes a line 1.08 μm high by 95 percent. This is per coating, independent of final polymer thickness after it is two to three times as thick as the feature. Photoimageable BCB 5 μm thick over an isolated 2.5-μm-high line planarizes larger linewidths much better than does polyimide not terminated by acetylene [24]. Table 6 gives such planarization by benzocyclobutene. By being planar, a dielectric has a constant, and usually smaller, thickness. This permits a smaller pitch and more levels, but fabricating the required stacked vias requires electroless plating or other complexity. The dielectric has thickness variations with interconnection line density. In general, a via may be unfilled or filled with metal, or be a plated-up post; stacked vias are denser than vias of nested steps.

Polyimide is the most widely used organic dielectric, but presents problems [22,24] in that it requires imidizing by ramping to 400°C, is degraded by H_2O uptake, and shrinks to have less planarization. Its precursor polyamic acid in a solvent is not sprayed or extruded but spun on, flinging off more material than remains. This material loss is expensive, particu-

Table 6. Planarization by benzocyclobutene (5 μm thick over a 2.5-μm-high line).

Isolated linewidth (μm)	Planarization (%)
5	91
10	83
15	70
33	50
100	24

larly for the larger areas and 10- to 15-μm finished thickness of MCMs. This precursor material must then be completely imidized to polyimide, releasing acidic H_2O, which corrodes Cu; compatible processing is complex. Later, precautionary bakeouts of absorbed H_2O are necessary. Most polyimide can notably withstand up to 400°C, and polyimide siloxane can withstand up to 450°C. Properties vary; modified types may lose chemical resistance. Some types are negatively photoimageable. Pre-imidized polyimide is not widely used. Imidization shrinks the thickness by more than 25 percent and often by 50 percent. Accordingly, patterns withdraw from the edges by a distance smaller than the shrinkage. The low solids content and large shrinkage permit only 30 percent or less planarization. Low-stress polyimide with low in-plane CTE has much higher z-axis $\varepsilon/\varepsilon_0$ and CTE.

Among common organic dielectrics, only the parylenes are vapor deposited. This vapor deposition is at or below room temperature and hence coats uniformly and very conformally. Parylenes are used as an outer coating and can be O_2-plasma patterned at a slow rate through a metal mask. The metal must later be etched without other materials being etched; one possibility is Ti removed by H_2O_2. H_2O uptake is a negligible 0.06 percent. Parylene-c is poly(chloro-para-xylylene), the polymer of $-CH_2-$(benzene-like C_6H_3Cl ring)$-CH_2-$. The substrate is soaked in its adhesion promoter solution, which may leave O in the film [25]. Then deposition is at room temperature in a vacuum of up to 10 Pa. Parylene-c melts at 280°C. Replacing the Cl with an H produces parylene-n, which has a phase transition at 220°C, melts at 405°C, and has a low $\varepsilon/\varepsilon_0$ of 2.65. It protects solder when deposited at least 3 μm thick on a chip that is flip-chip bonded by controlled-collapse chip-connection solder balls; solder's under-bump metallurgy achieves good adhesion, a diffusion barrier, and a solderable base of controlled wetting area [26]. The low permeability of parylene-n blocks O_2, H_2O, and CO_2 from corroding solder. During thermal cycling, parylene-n reduces shear strain from 3.7 to 2.9 percent, doubling the solder's lifetime.

Parylene-f withstands heat better than the other parylenes [25,27]. It is α α′ α″ α‴ poly-tetrafluoro-para-xylylene, the polymer of $-CF_2-$(benzene-like C_6H_4 ring)$-CF_2-$. It is polymerized as deposited at –30 to –20°C for good yield and adheres well. Vertical texturing starts at 350°C. A weblike microstructure develops at 425°C, as opposed to 350°C for parylene-n. Temperatures used in soldering and MCM repair reach 300 to 450°C, which parylene-f tolerates; it can withstand 480°C without losing weight. In 40 Pa of air, it densifies 4.2 percent at 250°C and 9.7 percent at 425°C. Its deposited volume resistivity is 1.3×10^{16} Ω-cm, its CTE is a smaller 2.7×10^{-5}/°C, and its $\varepsilon/\varepsilon_0$ of 2.38 is the lowest value of adhering candidate films. Stress for parylene-f as deposited is –10 MPa and after annealing at 350°C is 20 MPa, half that of parylene-n. Without an adhesion promoter, parylene-f adheres to dry Al and to wet or dry Si. Like parylene-n, its coating for a 1-μm-wide, 2-μm-deep trench was conformal and without pinholes. The outermost 100 nm is twice as hard, perhaps from shorter, denser polymer chains that crystallize easily. Crystallinity is initially low but, like that of parylene-c and parylene-n, increases much faster than the annealing tem-

perature increases. At 13 to 40 Pa of air, Cu diffuses into parylene-f as $3.5 \times 10^{-5} \exp(-1.14\ \text{eV}/kT)\ \text{cm}^2/\text{s}$, where k is Boltzmann's constant in electron volts per kelvin and T is temperature. This diffusion is modest below 350°C for MCM's larger thicknesses, and no diffusion barrier is usually required. Cr on parylene-n is a proven glue layer. Cr on parylene-f could possibly be a glue layer for and a diffusion barrier to Cu, to prevent Cu at temperatures above 350°C from delaminating. Cr on Al could be an adhesion layer for circuits passivated with parylene-f.

6. Difficulties with MCMs

The need for MCMs more advanced than hybrid circuits has increased over the years [6]. Although more chips give additional complexity within the MCM package, MCMs are gradually becoming established as a more standard packaging approach, rather than as custom packages. One requirement before MCMs gain widespread acceptance is the elimination of multiple repair cycles during the fabrication phase. Test standards, fixturing for testing unpopulated MCM substrates, and final testing must be developed. Detailed information about chips from suppliers, certainly more than test vectors, could help tame MCM diagnosis and repair. This would also aid fabrication in the long run.

Repairs, particularly of high-value MCMs, are often of interconnection lines; a laser can separate shorted lines or can be used in CVD of metal to repair lines [11]. A few vias that are open can be repaired by engineering-change wiring on expensive MCMs. Rework usually means replacement of the defective chip.

6.1 Testing

Adequate testing of chips and of MCMs is enormously important [28,29]. Testing requirements are time consuming and expensive. Testing systems must accommodate a complex MCM that accomplishes a new level of performance, function, and fabricated structure.

Basic chip testing by wafer probe includes static or low-frequency probing for minimal functionality. This may include hot chuck probing, voltage stress testing, and full testing for full functionality and any speed grading. A burn-in with electrical stressing accelerates early failures that later testing rejects, particularly for an advanced die with low yield. Full testing is usually the final step. Testing includes a boundary-scan test of interconnections and continuity, a functional test of full-speed functionality and device interactions, and an external I/O pin parametric test [30].

6.2 Known Good Dice (KGD)

The yield of an MCM is, at best, the product of the yield of each of its chips or dice. KGD are a difficult goal. KGD are widely agreed to be the largest obstacle to wide use of MCMs. KGD suitable for MCMs are more than just

tested bare chips. Genuine KGD are at least fully tested, all burned in, 100-percent proven to be good, undamaged by handling, and adequately described by geometric, electrical, thermal, supply, process, logic simulation, timing, and test-development data. KGD were and may still be difficult to obtain, especially outside a vertically integrated systems manufacturer that produces all the chips and its own MCM. Without the availability of KGD, an MCM with more than the few chips that are currently typical would tend to have a low yield.

Generally, it is not a good or economical approach to de-encapsulate chips packaged in epoxy. Chips are typically de-encapsulated by enclosed heated fuming nitric acid, a costly process that has a significant degrading effect on the chip.

Bare semiconductor chips (few are now KGD) might be at least 15 percent of production at the end of this decade [31,32]. Manufacturers such as Micron, Intel, National Semiconductor, IBM, Motorola, and Samsung are now selling some chips as at least partially KGD. Wafer-level burn-in might finally be developed to meet this requirement in future years and would reduce the piecework effort later. This approach would need to accommodate less chip variety than the currently available packaged chips. Test circuitry might be fabricated on the wafer around each chip. This built-in test (BIT) for each die would facilitate consistent chip testing at all levels of MCM assembly [9].

Testing of bare chips separated from the wafer is unattractively difficult. Ways to hold the dice during testing include soft connections, minimal packages, and temporary carriers. With temporary carriers, desoldering is rough, so that solder balls must be reformed at higher temperature. One can do chip-level burn-in and testing by automatically optically aligning and clamping the chip in a temporary carrier for testing [28]; neither this procedure nor handling is feasible with existing techniques. An alignable, reusable carrier and a reusable, gentle mechanical-only contact set have only recently been developed.

High-speed testing [28] is an additional difficulty. Current cantilever probe cards such as blade and epoxy ring probe cards give fewer than 400 connections and are slower than possible future membrane probe cards, flexible circuit interconnection sockets, and Si probe cards. Chips with solder-ball array contacts have more I/O connections than are currently available. A buckling beam contact is a vertical probe wire that curves when it touches a die pad. IBM's Cobra Probe fixture pre-curves the buckling beam to control the force. The pattern at both ends of the probe wire is that of the solder-ball array.

7. Design and CAD Requirements

Initial design should accommodate manufacturability, testing, repairability, performance, reliability, and cost. Computer-aided design (CAD), including simulation programs, has begun to appear for MCM interconnec-

tions and parasitic capacitance analysis. Industry standards aim for the required exchangeability of information [30]. An alliance functioning like a vertical integration between MCM industry sectors could improve the information depth, accuracy, usability, and cost. If great progress were made in establishing teamwork between industry sectors for experience, this could support the learning curve and lead to a positive perception of MCM. Thoroughly developed CAD would have a recommended methodology of design, containing cross sections and materials, and would be a useful starting point. The level of integration beyond the MCM could also be simulated. Complex MCMs must be designed for testability. For even the most popular MCM types, limited CAD usage and continual improvement of MCMs delay complete development of CAD.

8. Conclusions

This report provides an overview of MCMs and a discussion of some processing and materials. Generic common chip carrier designs do not seem to exist. All the MCM technology and repair techniques have tradeoffs and limitations. The capabilities of MCM-L/D and MCM-D are still improving, but development and standards are in an early stage; techniques are customized to circuit requirements. Greater volume production is needed, even for few-chip modules. Before making MCMs, an organization should carefully plan for its end needs and examine its abilities to achieve these.

References

1. G. Messner, I. Turlik, J. W. Balde, and P. E. Garrou, ed., *Thin Film Multichip Modules*, Intl. Soc. Hybrid Microelectr., Reston, VA (1992).

2. *Proc. Second Intl. Conf. Exhib. Multichip Modules*, Denver, CO, Intl. Soc. Hybrid Microelectr. and Intl. Electr. Packaging Soc. (1993).

3. *Proc. IEEE Multichip Module Conference* (IEEE Circ. Sys. Soc., IEEE Compon. Hybrids Manuf. Tech. Soc., IEEE Comp. Soc., IEEE Elec. Dev. Soc.), Santa Cruz, CA, IEEE Comp. Soc. Press (1992).

4. P. Lall and S. Bhagath, "An Overview of Multichip Modules," *Solid State Technol.* **36**, No. 9 (September 1993), 65.

5. G. Messner, I. Turlik, J. W. Balde, and P. E. Garrou, ed., *Thin Film Multichip Modules*, ch. 2, "Background to MCM Technology," Intl. Soc. Hybrid Microelectr., Reston, VA (1992).

6. R. Iscoff, "MCMs: Packaging's Final Frontier?," *Semiconductor Intl.* **14**, No. 10 (September 1991), 64.

7. G. Messner, I. Turlik, J. W. Balde, and P. E. Garrou, ed., *Thin Film Multichip Modules*, ch. 1, "Introduction," Intl. Soc. Hybrid Microelectr., Reston, VA (1992).

8. D. A. Doane and P. Franzon, "The Case for Multichip Modules," *Semiconductor Intl.* **17**, No. 4 (April 1994), 85.

9. R. Bone, D. Elwell, R. McBride, W. Schenet, and M. Stelling, "Understanding MCM Assembly and Testing," *Solid State Technol.* **37**, No. 10 (October 1994), 87.

10. L. Schaper, "Design of Multichip Modules," *Proc. IEEE* **80**, No. 12 (1992), 1955.

11. R. R. Tummala, "Multichip Packaging—A Tutorial," *Proc. IEEE* **80**, No. 12 (1992), 1924.

12. L. Economikos, "Laser System for Fine Pitch Tape Automated Bonding," *J. Vac. Sci. Technol. B* **12**, No. 4 (1994), 2394.

13. P. N. Dunn and Sun Microsystems, "Diamond-Copper-Silver Alloy Developed for MCM Substrates," *Solid State Technol.* **37**, No. 7 (July 1994), 36.

14. B. Besser, L. Bell, and D. Robinson, "MCM-L Approach Provides Cost-Effective Multichip Modules," Solid State Technol. **37**, No. 4 (April 1994), 49.

15. J.-P. Cazenave, "High-Density Interconnections with Thick-Film MCMs," *Solid State Technol.* **37**, No. 5 (May 1994), 47.

16. J. K. Hagge, "State-of-the-Art Multichip Modules for Avionics," *IEEE Trans. Compon. Hybrids Manuf. Tech.* **15**, No. 1 (1992), 29.

17. Booz-Allen and Hamilton, Inc., presentation, "Multichip Modules," to ARL at Adelphi, MD (10 November 1993).

18. T. G. Tessier, I. Turlik, G. M. Adema, D. Sivian, E. K. Yung, and M. J. Berry, "Process Considerations in Fabricating Thin Film Multichip Modules," *Intl. Electr. Packaging Symp. Proc.*, San Diego, Intl. Electr. Packaging Soc. (1989), 248, or reprint 290.

19. D. Burdeaux, P. Townsend, J. Carr, and P. Garrou, "Benzocyclobutene (BCB) Dielectrics for the Fabrication of High Density, Thin Multichip Modules," *J. Electr. Mater.* **19**, No. 12 (1990), 1357.

20. "Typical Properties of Cyclotene," brochure with bibliography of 65 articles, Dow Chemical Co.

21. R. H. Heistand, R. DeVellis, T. A. Manial, A. P. Kennedy, T. M. Stokich, P. H. Townsend, P. E. Garrou, T. Takahashi, G. M. Adema, M. J. Berry, and I. Turlik, "Advances in MCM Fabrication With Benzocyclobutene (BCB) Dielectric," *Intl. J. Microcircuits Electr. Pack.* **15**, No. 4 (1992), 183.

22. T. A. Cloud, M. R. Houston, and P. A. Kohl, "Processing and Performance of Gold MCM's," *IEEE Trans. Compon. Hybrids Manuf. Tech.* **16**, No. 7 (1993), 724.

23. A. Schiltz, "A Review of Planar Technologies for Multichip Modules," *IEEE Trans. Compon. Hybrids Manuf. Tech.* **15**, No. 2 (1992), 236.

24. P. Garrou, "Polymer Dielectrics for Multichip Module Packaging," *Proc. IEEE* **80**, No. 12 (1992), 1942.

25. S. Dabral, X. Zhang, X. M. Wu, G.-R. Yang, L. You, C. I. Lang, K. Hwang, G. Cuan, C. Chiang, H. Bakhru, R. Olson, J. A. Moore, T.-M. Lu, and J. F. McDonald, "$\alpha\,\alpha'\,\alpha''\,\alpha'''$ Poly-tetrafluoro-*p*-xylylene as an Interlayer Dielectric for Thin Film Multichip Modules and Integrated Circuits," *J. Vac. Sci. Technol. B* **11**, No. 5 (1993), 1825.

26. H. M. Tong, L. S. Mok, K. R. Grebe, H. L. Yeh, K. K. Srivastava, and J. T. Coffin, "Effects of Parylene Coating on the Thermal Fatigue Life of Solder Joints in Ceramic Packages," *IEEE Trans. Compon. Hybrids Manuf. Tech.* **16**, No. 5 (1993), 571; also "Parylene" brochure, Novatran Corp. and Union Carbide Corp.

27. L. You, G.-R. Yang, C.-I. Lang, J. A. Moore, P. Wu, J. F. McDonald, and T.-M. Lu, "Vapor Deposition of Parylene-F by Pyrolysis of Dibromotetrafluoro-*p*-xylene," *J. Vac. Sci. Technol. A* **11**, No. 6 (1993), 3047.

28. M. Begay, "Bare-Die Test Strategies for the MCM Market," *Solid State Technol.* **37**, No. 6 (June 1994), 65.

29. G. Messner, I. Turlik, J. W. Balde, and P. E. Garrou, ed., *Thin Film Multichip Modules*, ch. 13, "Testing: Known-Good ICs for MCM Assembly, Testing Assembled Multichip Modules Using Boundary-Scan and Built-In Self-Test, Substrate Interconnection Verification," Intl. Soc. Hybrid Microelectr., Reston, VA (1992).

30. S. C. Tasker and Z. Sekulic, "Adopting Multichip-Module Technology," *Electronic Design* **42**, No. 13 (27 June 1994), 153.

31. L. Peters, "Tackling the Challenges of KGD," *Semiconductor Intl.* **17**, No. 6 (June 1994), 60.

32. D. Maliniak, "Known-Good Die Poised to Take Off," *Electronic Design* **42**, No. 23 (21 November 1994), 55.

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